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Computer Engineering Department

DIGITAL CIRCUITS EXAM QUESTIONS

QUESTION 1:

a. A and B are two 8-bit, **signed**, binary integers. B is given as B=1001 1101. If we perform the operation A-B using the **2's complement** system, overflow occurs and the most significant bit of the 8-bit result is 1.

i) What is the sign of A (positive or negative)? Why?

ii) Write the smallest possible integer A that can constitute this situation (result and overflow).

b. A and B are two 8-bit, **unsigned**, binary integers. After the operation A-B using the **2's complement** system, the obtained result is a 9-bit number: 1 1001 0110.
Which is true A>B or A<B? Why?

QUESTION 2:

a. E and F are two expressions, which do not include the literal a. Write the expression in PoS form, of which E+F is the consensus term respect to a.
Note: To show complements put a dash over literals, such as $\bar{a}$.

b. Write the consensus theorem for the obtained expression in PoS form (above) and prove it (in PoS form) using the axioms and theorems of the Boolean algebra.

c. Minimize the given expression using the consensus theorem and other necessary theorems of the Boolean algebra. z = ab'c + ab + acd + a'b
To show complements put a dash over literals, such as $\bar{a}$.
Implement the minimized expression using **only** 2-input NAND gates.

QUESTION 3:

a) Minimize the following function using axioms and theorems.
f(A,B,C,D)=A'B'CD+AB'CD+AC'D+AC'D'+A'B'CD'+ABCD+ACD'

b) Write the simplest expression for the following function as product of sums. Draw the Karnaugh diagram. You do not need to use prime implicant chart.
$f(A,B,C,D)=U_1(0,1,2,3,6,8,9,10,11,14)+U_\Phi(12,15)$

QUESTION 4:

Expression of a function f(a,b,c,d) is given in 2nd canonical form that includes 6 maxterms.
f(a,b,c,d)= (a+b+c+d′)(a+b′+c+d′)(a′+b′+c+d)(a′+b′+c+d′)(a′+b′+c′+d)(a′+b+c+d′)

a. Draw the Karnaugh map of the function f(a,b,c,d) and find all prime implicants.
b. Find all prime implicants of the **complement** ($\bar{f}$(a,b,c,d)) of the function using the Quine-McCluskey method.

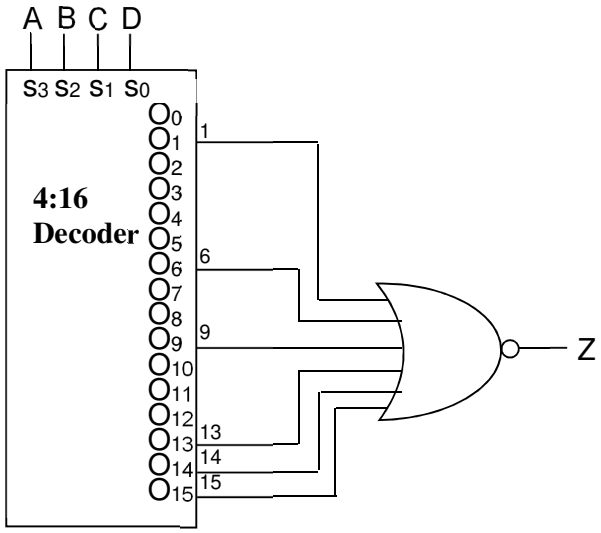
QUESTION 5:

a. Find the sufficient base with the lowest cost (minimal covering sum) for the following chart. Calculate the cost. Show your work.

	0	**2**	**4**	**5**	**7**	**8**	**10**	**11**	**13**	**14**	**Cost**
A	X									X	6
B	X			X	X			X		X	8
C		X		X		X	X				8
D		X		X			X				8
E					X	X	X	X	X	X	10
F			X		X				X	X	10

QUESTION 6:

An incomplete logic function Z=f(A,B,C,D) is implemented by using a 4:16 decoder and a **NOR** gate. Don't care input values (A,B,C,D) is:**1100**



a. Draw the Karnaugh map of the function and find all prime implicants.
To show complements put a dash over literals, such as $\bar{a}$.

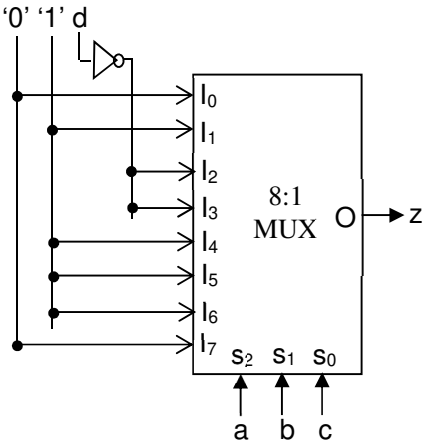
b. Construct the prime implicant chart.
The cost criteria: 2 units for each variable and 1 unit for each complement sign.

c. Simplify the prime implicant chart and find the cheapest expression of the function.

QUESTION 7:

The given combinational circuit has four inputs (a,b,c,d) and one output (z).

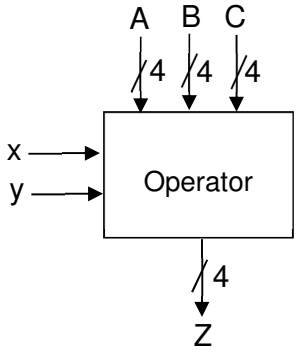
a. Construct the truth table of this circuit and write the expression of the logical function z=f(a,b,c,d) in 1st canonical form.
b. Minimize the expression using axioms and theorems of the Boolean algebra.
c. Design and draw the same circuit using a 4:16 decoder and other necessary logic gates.



QUESTION 8:

a) The combinational circuit (Operator) shown on right performs operations on three 4-bit unsigned integers $A=A_3\ A_2\ A_1\ A_0$, $B=B_3\ B_2\ B_1\ B_0$ and $C=C_3\ C_2\ C_1\ C_0$. The type of the operation is determined by the inputs x and y as follows:

x y	Operation
0 0	Z=A
0 1	Z=B
1 0	Z=A+B
1 1	Z=A+C



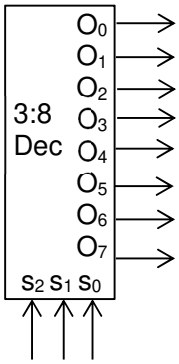
Design and draw this combinational circuit (Operator) using one parallel adder, multiplexers and other necessary logic gates.

QUESTION 9:

The block diagram of a 3:8 decoder is shown on the right.

Design and draw **a 3:8 decoder** using only **two 2:4 decoders** with "enable - EN" inputs and **one NOT** gate.

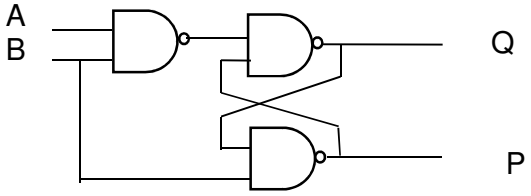
Fully label all inputs and outputs (including those on the decoders).



QUESTION 10:

Analyze the given circuit by applying different input values and show that this circuit can be used as a memory unit.

Derive the next state equation for Q as $Q(t+1)=f(A,B,Q(t))$.



QUESTION 11:

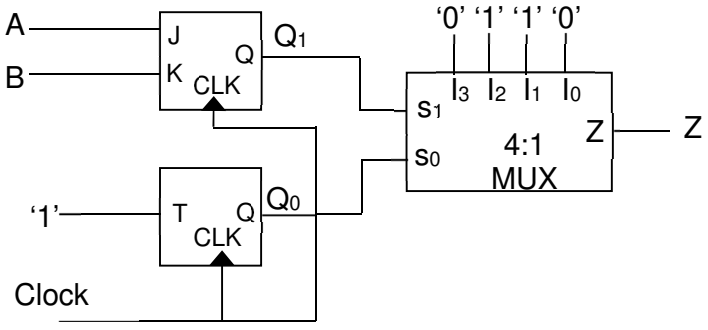
a. Analyze the given clocked synchronous circuit with two inputs (A,B) and one output (Z) and construct the State/Output table.

Note: Q_1 is the most significant state variable and Q_0 is the least significant one.

Show steps shortly, how you created the table.

Draw the state diagram of the circuit.

b. Design and draw the circuit with the same behavior (as in a.) by using D flip-flops and **only** 2-input NAND gates.



QUESTION 12:

A clocked synchronous circuit with one input (X) and one output (Z) will be designed using the **Moore model**. Whenever the total number of "1"s received at input X during the positive edges of the clock signal is odd and greater than 2 (3, 5, 7, …), the output Z will be "1", otherwise "0". The "1"s at the input X don't need to be successive.

Example of input and output sequences:

X = 1 1 1 0 0 1 0 1 0 1 0

Z = 0 0 1 1 1 0 0 1 1 0 0

a. Draw the state diagram and construct the State/Output table of the circuit.

b. Implement and draw the circuit using positive edge triggered **JK** flip-flops and other necessary logic gates.

QUESTION 13:

The internal structure of a CMOS logic gate is given on the right.

Examine the given circuit.

Make a table showing the states (on/off) of the transistors (Q_x).

Write the expression for the function Z=f(A).